

Office Action Summary

Application No.	08/650,719	Applicant(s)	Mailoux et al
Examiner	H. Kim	Group Art Unit	2751

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

Responsive to communication(s) filed on 9/30/99

This action is **FINAL**.

Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

Claim(s) 1-9, 33-35, 46, 48-49, 50 + 59-64 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

Claim(s) _____ is/are allowed.

Claim(s) 1-9, 33-35, 46, 48-50 + 59-64 is/are rejected.

Claim(s) _____ is/are objected to.

Claim(s) _____ are subject to restriction or election requirement.

Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

The proposed drawing correction, filed on _____ is approved disapproved.

The drawing(s) filed on _____ is/are objected to by the Examiner.

The specification is objected to by the Examiner.

The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

All Some* None of the CERTIFIED copies of the priority documents have been received.

received in Application No. (Series Code/Serial Number) _____.

received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

Attachment(s)

Information Disclosure Statement(s), PTO-1449, Paper No(s). _____ Interview Summary, PTO-413

Notice of References Cited, PTO-892 Notice of Informal Patent Application, PTO-152

Notice of Draftsperson's Patent Drawing Review, PTO-948 Other _____

Office Action Summary



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

MS

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
-----------------	-------------	----------------------	---------------------

08/650,719 05/20/96 MAILLLOUX

J 95-0653

021186 LM02/1215
SCHWEGMAN LUNDBERG WOESSNER & KLUTH
P O BOX 2938
MINNEAPOLIS MN 55402

EXAMINER

KIM, H

ART UNIT	PAPER NUMBER
----------	--------------

2751

30

DATE MAILED:

12/15/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Detailed Action

Continued Prosecution Application

1. The request filed on 9/30/99 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 08/650,719 is acceptable and a CPA has been established. An action on the CPA follows.

2. Claims 1-9, 33-35, 46, 48-50 and 59-64 are presented for examination. Claims 59-64 have been added by the amendment. This office action is in response to the Amendment filed on 9/30/99.

3. The status of the related U.S. applications or patents should be updated and/or included as appropriate in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification, if any. (e.g., U.S. Patent Application Serial No. #####,### filed Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number #####,###, filed on December 01, 1990, now abandoned; ...etc.)

Claim Objections

4. Claims are objected to because of the following informalities:
As to claim 46, it appears that burst and pipelined should be swapped, see originally filed

claim 47.

As to claim 61, it is unclear to the Examiner how to generate at least one subsequent internal address patterned after the initial external address while in the pipelined mode of operation. It appears that there is no support in the specification.

5. It appears that newly submitted claim 62-64 directed to an invention that is independent or distinct from the invention originally claimed.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 62-64 should be withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

6. Claims 59-62 are objected to under 37 CFR 1.75(b) as not substantially differing from claims 1-9, 33-35, 46, and 50.

The claims as written do not appear to be substantially different or to provide substantially different patent protection.

Applicants are required to 1) cancel the objected to claims,(2) amend the claims so that they are substantially different from any other claims, or (3) provide sufficient reasons why the claims as presently written are substantially different or provide substantially different patent protection. Also claims 63 is objected to under 37 CFR 1.75(b) as not substantially differing

from claim 64.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-9, 33-35, 46, 48-50, and 59-64 are rejected under 35 USC § 103(a) as being unpatentable over Manning, U.S. Patent 5,610,864 in view of Ryan, U.S. Patent 5,966,724.

As to claim 1, Manning discloses an asynchronously accessible storage device (Fig. 1 and EDO constitutes asynchronous memory, col. col. 6 lines 14-16) comprising mode circuitry to select between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and an EDO mode (col. 6 lines 14-26); and circuitry operable in either the burst mode or the EDO mode coupled to the mode selection circuitry and configure to select between two modes.(Fig. 1 Ref. 40 and col. 6 lines 14-16).

Although Manning discloses the option of switching between burst EDO and standard EDO modes of operation (col. 6 lines 14-16), a pipelined architecture (col. 5 lines 42-44), and in a pipelined architecture the overall throughput of the memory approaches one access per cycle (col. 5 lines 45-50), Manning does not specifically disclose the mode circuitry configured to select between a burst mode and an pipelined mode. However, it was well known in the memory art that the mode circuitry to select between the burst mode (col. 4 lines 25-26) and the pipelined mode (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). Pipelined is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput by providing data once per memory access cycle.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of the mode circuitry to select between the burst mode and the pipeline mode of Ryan into the invention of Manning because Ryan states that it would achieve high data throughput in the memory.

As to claim 50, Manning further discloses a microprocessor (Fig. 11 Ref. 112). Manning also disclose a system clock (col. 8 line 46) in the microprocessor to operate the processor.

As to claim 2, Ryan further discloses the burst mode and the pipelined mode are EDO modes of operation (col. 4 lines 21-26).

As to claim 3, Ryan further discloses the pipelined mode is an EDO mode (col. 4 line 24).

As to claim 4, Manning further discloses the burst mode is and EDO mode (col. 6 line 15).

As to claim 5, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 6, Manning further discloses the mode circuitry includes at least one counter for incrementing the address (Fig. 1 Ref. 26 and col 5 lines 51-62).

As to claim 7, Manning further discloses the mode circuitry includes receiving an external address (Fig. 1 Ref. 16 and col. 4 lines 16-28).

As to claim 8, Manning further discloses the mode circuitry includes a buffer, the buffer for storing an address (Fig. 1 Refs. 18, 22, and 30).

As to claim 9, Manning further discloses the mode circuitry includes multiplexed device for providing an internally generated address to the storage device (Fig. 1 Refs. 26 and 30 and col. 5 lines 51-62, selection of external or internal address reads on this limitation).

As to claims 33 and 59, Manning discloses a method for accessing a storage device (Fig. 1), comprising: receiving a first address to the storage device (Fig. 2 ROW); selecting between an asynchronously accessible (Fig. 1 and EDO constitutes asynchronous operation, col. col. 6 lines 14-16) burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and an EDO mode (col. 6 lines 14-26) of operations of the storage device; selecting between outputting information from the storage device and inputting to the storage device (Fig. 2 /WE, read and write operations read on this limitation); obtaining a second address to the storage device (Fig. 2 /COL), and asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second addresses (Fig. 2, DQ).

Although Manning discloses the option of switching between burst EDO and standard EDO modes of operation (col. 6 lines 14-16), a pipelined architecture (col. 5 lines 42-44), and in a pipelined architecture the overall throughput of the memory approaches one access per cycle (col. 5 lines 45-50), Manning does not specifically disclose the step of selecting between a burst mode and an pipelined mode. However, it was well known in the memory art that the step of selecting select between the burst mode (col. 4 lines 25-26) and the pipelined mode (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). Pipelined is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput by providing data once per memory access cycle.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of the step of selecting between the

burst mode and the pipeline mode of Ryan into the invention of Manning because Ryan states that it would achieve high data throughput in the memory.

As to claim 34, Manning further discloses a step of switching between the pipelined mode and burst mode (col. 6 lines 14-16 and col. 5 lines 42-50).

As to claim 35, Manning further discloses the second address is an external address (Fig. 1 Refs 16 and 30).

As to claim 60, Manning further discloses selecting between outputting information from the storage device and inputting to the storage device (Fig. 2 /WE, read and write operations read on this limitation)

As to claim 46, Manning discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes asynchronous operation, col. 6 lines 14-16), comprising: selecting a burst mode of operation (col. 6 lines 14-26 and col. 7 lines 43-54); providing a new external address (Fig. 2 COL); switching mode to a non-burst (col. 6 lines 31-32 and col. 6 lines 14-26); providing an initial external addresses (Fig. 2 COL); and generating internal addresses (Fig. 1 Ref. 26, col. 4 lines 48-49).

Although Manning discloses the option of switching between burst EDO and standard EDO modes of operation (col. 6 lines 14-16), a pipelined architecture (col. 5 lines 42-44), and in a

pipelined architecture the overall throughput of the memory approaches one access per cycle (col. 5 lines 45-50), Manning does not specifically disclose the step of switching mode to an pipelined mode. However, it was well known in the memory art that the step of switching mode to the pipelined mode (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). Pipelined is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput by providing data once per memory access cycle.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of the step of switching modes to the pipeline mode of Ryan into the invention of Manning because Ryan states that it would achieve high data throughput in the memory.

As to claims 48 and 49, Manning further discloses column, row, application, fixed access based switching (Fig. 1 Refs. 38 and 40) for the burst mode. Ryan further discloses column, row, application, fixed access based switching (Fig. 1 Refs. 38 and 40) for the pipelined mode.

As to claim 61, Manning discloses a method for accessing several different locations in an asynchronously a storage device (Fig. 1 and EDO constitutes asynchronous operation, col. col. 6 lines 14-16), comprising: selecting a non-burst mode of operation (col. 6 lines 31-32 and col. 6 lines 14-26); providing an initial address (Fig. 2 COL); generating internal addresses (Fig. 1 Ref.

26, col. 4 lines 48-49); switching mode to a burst mode of operation (col. 6 lines 14-26 and col. 7 lines 43-54); and providing a new external address (Fig. 2 COL).

Although Manning discloses the option of switching between burst EDO and standard EDO modes of operation (col. 6 lines 14-16), a pipelined architecture (col. 5 lines 42-44), and in a pipelined architecture the overall throughput of the memory approaches one access per cycle (col. 5 lines 45-50), Manning does not specifically disclose the step of switching mode to an pipelined mode. However, it was well known in the memory art that the step of switching mode to the pipelined mode (col. 4 lines 21-25) and providing an external addresses when switching the mode (col. 4 lines 35-39, if BC is high constitutes that switching between pipeline and burst modes and col. 4 lines 25-27) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). Pipelined is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput by providing data once per memory access cycle.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of the step of switching modes to the pipeline mode of Ryan into the invention of Manning because Ryan states that it would achieve high data throughput in the memory.

As to claim 62, Ryan further discloses the step of selecting an external address path if the pipeline (col. 4 lines 21-24) and selecting an internal addresses path if the burst mode (col. 4 lines 25-27).

As to claims 63 and 64, *Manning* further discloses an array of memory cells (col. 4 lines 13-15).

Response to Amendment

8. Applicant's arguments with respect to claims 1-9, 33-35, 46, 48-5, and 59-64 have been considered but are deemed to be persuasive.

Applicant's argument on page 4 middle that the reference does not disclose a mode circuitry to select between a burst mode and a pipeline modes of operations is not considered persuasive. Although *Manning* discloses option of switching between burst EDO and standard EDO modes of operation (col. 6 lines 17-40) and "other memory architecture applicable to the current invention includes a pipelined architecture" (col. 5 lines 43-45), Ryan discloses a mode circuitry to select between a burst mode and a pipeline mode of operation (col. 4 lines 20-27) for the purpose of high data throughput (abstract lines 8-9). Therefore, broadly written claims are disclose by the references cited.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. USP 5966724, 19991012, Synchronous memory device with dual page and burst mode operations, Ryan, Kevin J.
2. US 5752269, 19980512, Pipelined microprocessor that pipelines memory requests to an external memory, Divivier, Robert J. , et al..

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

11. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

12. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can

normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

15. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

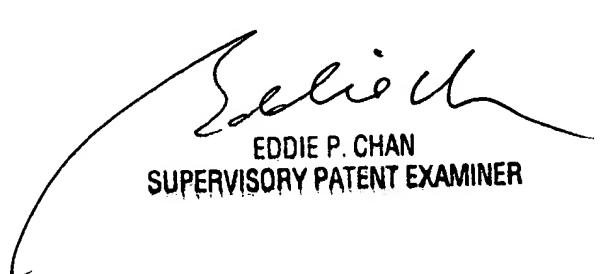
(703) 308-9051-2, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label
"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

11/8
HK
Patent Examiner
December 8, 1999


EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER